Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 5. (Canceled)

6. (Amended) A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a metal layer on ~~the~~ said high-k gate dielectric layer~~, the metal layer being less than about 100 angstroms thick~~;

forming a masking layer on ~~the~~ said metal layer, exposing part of ~~the~~ said metal layer; and

applying a wet etch chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a chelating agent;

wherein, ~~to remove the~~ said exposed part of ~~the~~ said metal layer is removed from ~~the~~ said high-k gate dielectric layer by said chelating agent; and ~~without removing more than about 100 angstroms of the metal layer from beneath the masking layer;~~

wherein, said chelating agent has a diameter that exceeds the thickness of said metal layer.

7. (Amended) The method of claim 6 wherein ~~the~~ said metal layer comprises a material selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, a metal carbide, and a conductive metal oxide.

8. (Amended) The method of claim 6 wherein ~~the~~ said high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

9. (Amended) The method of claim 6 wherein ~~the~~ said masking layer comprises polysilicon.

10. (Amended) The method of claim 6 wherein ~~the~~ said metal layer is between about 25 angstroms and about 50 angstroms thick.

11. (Amended) A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a metal layer on ~~the~~ said high-k gate dielectric layer, ~~the~~ said metal layer being between about 25 angstroms and about 50 angstroms thick;

forming a polysilicon containing layer on ~~the~~ said metal layer;

removing a first portion of ~~the~~ said polysilicon layer to expose part of ~~the~~ said metal layer; and

applying a wet etch chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a chelating agent to remove ~~the~~ said exposed part of ~~the~~ said metal layer from ~~the~~ said high-k gate dielectric layer; ~~without removing more than about 100 angstroms of the metal layer from beneath the polysilicon containing layer;~~

wherein, said chelating agent has a diameter that exceeds the thickness of said metal layer.

12. (Amended) The method of claim 11 wherein ~~the~~ said high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

13. (Amended) The method of claim 11 wherein ~~the~~ said metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV.

14. (Amended) The method of claim 11 wherein ~~the~~ said metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV.

15. (Amended) The method of claim 11 wherein ~~the~~ said chelating agent is a hexa-dentate chelating agent that is selected from the group consisting of carboxylic acid based chelating agents, phosphonic acid based chelating agents, and phenol derivatives.

16. (Amended) A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate, ~~the~~ said high-k gate dielectric layer comprising a material selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide;

forming a first metal layer on ~~the~~ said high-k gate dielectric layer, ~~the~~ said first metal layer being between about 25 angstroms and about 50 angstroms thick;

removing a first portion of ~~the~~ said first metal layer;

forming a second metal layer on ~~the~~ said high-k gate dielectric layer, ~~the~~ said second metal layer being between about 25 angstroms and about 50 angstroms thick, a first portion of ~~the~~ said second metal layer covering the remaining portion of ~~the~~ said first metal layer and a second portion of ~~the~~ said second metal layer covering ~~the~~ said high-k gate dielectric layer;

forming a polysilicon containing layer on ~~the~~ said second metal layer;

removing a ~~first~~ portion of ~~the~~ said polysilicon layer selectively to ~~the~~ said second metal layer to expose part of ~~the~~ said second metal layer; and

removing the exposed part of ~~the~~ said second metal layer and the underlying part of ~~the~~ said first metal layer selectively to ~~the~~ said high-k gate dielectric layer by exposing ~~the~~ said second metal layer and ~~the~~ said first metal layer to a wet

chemistry that comprises an aqueous solution that includes between about 0.5 and about 5.0 moles/liter of a hexa-dentate chelating agent that is selected from the group consisting of carboxylic acid based chelating agents, phosphonic acid based chelating agents, and phenol derivatives;

wherein, said hexa-dentate chelating agent has a diameter that exceeds the combined thickness of said first and said second metal layers.

17. (Amended) The method of claim 16 wherein ~~the~~ said first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and serves as a gate electrode for an NMOS transistor, and ~~the~~ said second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and serves as a gate electrode for a PMOS transistor.

18. (Amended) The method of claim 16 wherein ~~the~~ said first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and serves as a gate electrode for a PMOS transistor, and ~~the~~ said second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, comprises a material that is selected from the group consisting of hafnium,

zirconium, titanium, tantalum, aluminum, and a metal oxide, and serves as a gate electrode for an NMOS transistor.

19. (Amended) The method of claim 16 wherein less than about 100 angstroms of ~~the~~ said second metal layer and the underlying part of ~~the~~ said first metal layer are removed from beneath ~~the~~ said polysilicon containing layer, when the exposed part of ~~the~~ said second metal layer and the underlying part of ~~the~~ said first metal layer are removed selectively to ~~the~~ said high-k gate dielectric layer.

20. (Amended) The method of claim 19 wherein less than about 50 angstroms of ~~the~~ said second metal layer and the underlying part of ~~the~~ said first metal layer are removed from beneath ~~the~~ said polysilicon containing layer.

21. (New) A method comprising:

forming a metal layer on a substrate, said metal layer having a thickness;

forming a mask on said metal layer wherein said mask exposes a portion of said metal layer; and

applying a wet etchant that comprises an active ingredient to remove said exposed portion of said metal layer from said substrate;

wherein, said active ingredient has a diameter that exceeds said thickness of said metal layer.

22. (New) The method of claim 21 wherein said metal layer is between about 25 angstroms and about 50 angstroms thick.

23. (New) The method of claim 22 wherein said metal layer comprises a material selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, a metal carbide, and a conductive metal oxide.

24. (New) The method of claim 23 wherein said active ingredient comprises a chelating agent selected from the group consisting of carboxylic acid based chelating agents, derivatives of phenol, and phosphonic acid based chelating agents.

25. (New) A method comprising:

forming a metal layer on a substrate or a high-k gate dielectric layer, said metal layer having a thickness;

forming a mask on said metal layer wherein said mask exposes a portion of said metal layer; and

applying a wet etchant that comprises an active ingredient to remove said exposed portion of said metal layer from said substrate;

wherein, said active ingredient has a diameter that exceeds said thickness of said metal layer;

thereby preventing said active ingredient from significantly undercutting said metal layer underneath said masking layer.

26. (New) The method of claim 25 wherein said undercut is less than 100 angstroms.

27. (New) The method of Claim 26 wherein said undercut is less than 100 angstroms, regardless of the duration of application of said wet etch chemistry.

28. (New) The method of claim 25 wherein said metal layer is between about 25 angstroms and about 50 angstroms thick.

29. (New) The method of claim 28 wherein said metal layer comprises a material selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, a metal carbide, and a conductive metal oxide.

30. (New) The method of claim 25 wherein said high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.